C.) REMARKS

This Response is filed in response to the Office Action dated November 9, 2007.

Upon entry of this Response, claims 1-37 will be pending in the Application.

In the outstanding Office Action, the Examiner rejected claims 1-3, 9, 10, 12-15, 19, 20, 26, 27 and 29-36 under 35 U.S.C. 102(e) as being anticipated by Rahman et al. (U.S. Patent Application Publication No. 2004/0160201); and rejected claims 4-8, 11, 16-18, 21-25, 28 and 37 under 35 U.S.C. § 103(a) as being unpatentable over Rahman et al. (U.S. Patent Application Publication No. 2004/0160201 in view of Mokrytzki et al. (U.S. Patent No. 3,781,615) or Maurio et al. (U.S. Patent No. 6,118,932) or Duba et al. (U.S. Patent No. 6,101,109).

Rejection under 35 U.S.C. 102

The Examiner rejected claims 1-3, 9, 10, 12-15, 19, 20, 26, 27 and 29-36 under 35 U.S.C. 102(e) as being anticipated by Rahman et al. (U.S. Patent Application Publication No. 2004/0160201), hereafter referred to as "Rahman."

Specifically, the Examiner stated that

> Rahman et al show in figures 1-2 a plurality of inverters electrically connected in parallel to a DC link stage(206, 208). Rahman et al show in figures 1-6 that the controllers 224 and 264 generate CLK signals to the inverters. Rahman et al disclose at paragraph [0006] a method for reducing the power bus ripples of a multiple inverter system. Rahman et al further disclose at paragraph [0035] the RMS ripple current for the center based interleaved scheme and the leading and lagging edge coincident scheme to reduce RMS ripple current at the DC link stage.

Applicant respectfully traverses the rejection of claims 1-3, 9, 10, 12-15, 19, 20, 26, 27 and 29-36 under 35 U.S.C. 102(e).

Rahman, as understood, is directed to a multiple inverter system for a vehicle having a battery and a capacitor coupled in parallel to the battery. A first inverter is coupled to the battery and is adapted to drive a first motor. A first controller has an output coupled to the first inverter and provides a first pulse width modulated signal that is modulated in relation to a first clock signal. A second inverter is coupled to the battery and is adapted to drive a second motor. A second controller has an input for receiving a synchronization signal from the first controller, and

an output coupled to the second inverter for providing a second pulse width modulated signal that is modulated in relation to a second clock signal. The second controller uses the synchronization signal to generate the second clock signal having a predetermined relationship with respect to the first clock signal.

In contrast, independent claim 1, as amended, recites a method of controlling a variable speed drive having a converter stage, a DC link stage, and an inverter stage, the method comprising: providing an inverter stage having a plurality of inverters electrically connected in parallel to a DC link stage, each inverter of the plurality of inverters being configured to power a corresponding load; generating a switching signal for each inverter of the plurality of inverters with a plurality of modulators, the switching signal being operable to activate and deactivate the inverter to obtain a preselected output power and a preselected output frequency from the inverter, wherein generating a switching signal comprises: providing a common input signal to the plurality of modulators; and providing a phase shifted or time shifted input signal to each modulator of the plurality of modulators, wherein the phase shifted or time shifted input signal for one of the modulators being shifted relative to the corresponding input signal provide to the other modulators; and interleaving the switching signals for each inverter of the plurality of inverters to reduce RMS ripple current at the DC link stage.

Independent claim 13, as amended, recites a method of controlling a variable speed drive having a converter stage, a DC link stage, and an inverter stage, the method comprising: providing an inverter stage having a plurality of inverters electrically connected in parallel to a DC link stage, each inverter of the plurality of inverters being configured to power a corresponding load; generating a switching signal for each inverter of the plurality of inverters, the switching signal being operable to activate and deactivate the inverter to obtain a preselected output power and a preselected output frequency from the inverter, wherein generating a switching signal comprises providing a modulator to generate a single switching signal; and interleaving the switching signals for each inverter of the plurality of inverters to reduce RMS ripple current at the DC link stage, wherein interleaving the switching signals for each inverter of the plurality of inverters comprises: providing the single switching signal to one inverter of the plurality of inverters; and delaying the single switching signal by predetermined amounts before

providing the delayed single switching signals to the remaining inverters of the plurality of inverters.

Independent claim 14 recites a method of controlling a variable speed drive having a converter stage, a DC link stage, and an inverter stage, the method comprising the steps of: providing a converter stage having an active converter connected to a DC link stage; providing an inverter stage having at least one inverter electrically connected in parallel to the DC link stage; generating a first switching signal for the active converter, the first switching signal being operable to activate and deactivate the active converter to generate a preselected DC voltage at a DC link stage; generating a second switching signal for the at least one inverter, the second switching signal being operable to activate and deactivate the at least one inverter to obtain a preselected output power and preselected output frequency from the at least one inverter; and interleaving the first switching signal and the second switching signal to reduce RMS ripple current at the DC link stage.

Independent claim 19, as amended, recites a variable speed drive comprising: a converter stage to convert an AC voltage to a DC voltage, the converter stage being configured to be electrically connectable to an AC power source; a DC link stage to filter and store energy from the converter stage, the DC link stage being electrically connected to the converter stage; an inverter stage comprising a plurality of inverters electrically connected in parallel to the DC link stage, each inverter of the plurality of inverters being configured to convert a DC voltage to an AC voltage to power a corresponding load; a control system to control operation of the inverter stage, the control system comprising a plurality of modulators configured to generate switching signals for each inverter of the plurality of inverters, the control system being configured to provide a common input signal to the plurality of modulators and a phase shifted or time shifted input signal to each modulator of the plurality of modulators, the phase shifted or time shifted input signal for one of the modulators being shifted relative to the corresponding input signal provided to the other modulators; and wherein the switching signals for each inverter of the plurality of inverters are interleaved with the switching signals for the other inverters of the plurality of inverters.

Independent claim 31, as amended, recites a chiller system comprising: a first refrigerant circuit, the first refrigerant circuit comprising a first compressor driven by a first motor, a first condenser and a first evaporator connected in a closed refrigerant loop; a second refrigerant circuit, the second refrigerant circuit comprising a second compressor driven by a second motor, a second condenser and a second evaporator connected in a closed refrigerant loop; a variable speed drive comprising: a converter stage to convert an AC voltage to a DC voltage, the converter stage being configured to be electrically connectable to an AC power source; a DC link stage to filter and store energy from the converter stage, the DC link stage being electrically connected to the converter stage; and an inverter stage comprising a first inverter and a second inverter each electrically connected in parallel to the DC link stage, the first inverter being configured to convert a DC voltage to an AC voltage to power the first motor, and the second inverter being configured to convert a DC voltage to an AC voltage to power the second motor; a control system to control operation of the variable speed drive, the control system comprising a first modulator configured to generate switching signals for the first inverter and a second modulator configured to generate switching signals for the second inverter, the control system being configured to provide a common input signal to both the first modulator and the second modulator and a phase shifted or time shifted input signal to the first modulator and the second modulator, the phase shifted or time shifted input signal for one of the modulators being shifted relative to the corresponding input signal for the other modulator; and wherein the switching signals for the first inverter are interleaved with the switching signals for the second inverter to reduce an RMS ripple current in the DC link stage.

The examiner is reminded that "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)." *See* Manual of Patent Examining Procedure, 8th Edition, Revision 6 (MPEP), Section 2131.

In addition, "'[t]he identical invention must be shown in as complete detail as is contained in the ... claim.' *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." *See* MPEP, Section 2131.

Several of the features recited by Applicant in independent claims 1, 19 and 31 are not disclosed by Rahman. Rahman does not disclose providing a common input signal to the plurality of modulators and providing a phase shifted or time shifted input signal to each modulator of the plurality of modulators, wherein the phase shifted or time shifted input signal for one of the modulators being shifted relative to the corresponding input signal provided to the other modulators as recited by Applicant in independent claim 1 and similarly recited in claims 19 and 31. The system in Rahman does not disclose that the controllers are provided with a common signal and a phase shifted or time shifted signal to generate switching signals. The system in Rahman discloses only the use of clock signals to control the generation of switching signals, which clock signals are not provided to both controllers, i.e., a common signal, nor are the clock signals phase shifted or time shifted before being provided to a controller. In Rahman, switching signals are generated by a master controller that receives a clock signal and a slave controller that receives a processor sync signal from the master controller to generate a clock signal that is used by the slave controller. Thus, Applicant submits that the system in Rahman does not recite the providing of both a common input signal and a phase shifted or time shifted signal to generate the switching signals.

Furthermore, with regard to claims 19 and 31, Rahman does not disclose a converter stage to convert and AC voltage to a DC voltage as recited by Applicant. The system in Rahman does not disclose any type of converter stage and specifically discusses working from a battery, thereby precluding the need for a converter stage. Additionally, with regard to claim 31, Rahman does not disclose a first refrigerant circuit and a second refrigerant circuit. The system in Rahman does not disclose any refrigerant circuits and specifically is directed to automotive applications thereby precluding the presence of any refrigerant circuits.

Thus, since Rahman does not disclose all of the limitations recited in independent claims 1, 19 and 31, Applicant respectfully submits that Rahman does not anticipate Applicant's invention as recited in independent claims 1, 19 and 31.

With regard to claim 13, Rahman does not disclose interleaving the switching signals for each inverter of the plurality of inverters by delaying the single switching signal by predetermined amounts before providing the delayed single switching signals to the remaining

inverters of the plurality of inverters as recited by Applicant. The system in Rahman does not disclose the generation of only a single switching signal for the multiple inverters and specifically discusses the use of a corresponding controller to provide switching signals to each inverter. The Examiner is specifically requested to identify where in Rahman the generation of only one switching signal to be used for multiple inverters is disclosed. Thus, since Rahman does not disclose all of the limitations recited in independent claim 13, Applicant respectfully submits that Rahman does not anticipate Applicant's invention as recited in independent claim 13.

With regard to claim 14, Rahman does not disclose providing a converter stage having an active converter connected to a DC link stage and generating a first switching signal for the active converter as recited by Applicant. The system in Rahman does not disclose any type of converter stage and specifically discusses working from a battery, thereby precluding the need for a converter stage. Furthermore, since Rahman does not disclose a converter stage, Rahman cannot disclose interleaving the first switching signal (for the active converter) and the second switching signal (for the at least one inverter) to reduce RMS ripple current at the DC link stage as recited by Applicant in claim 14. Thus, since Rahman does not disclose all of the limitations recited in independent claim 14, Applicant respectfully submits that Rahman does not anticipate Applicant's invention as recited in independent claim 14.

Therefore, for the reasons given above, independent claims 1, 13, 14, 19 and 31 are believed to be distinguishable from Rahman and therefore are not anticipated nor rendered obvious by Rahman.

Dependent claims 2-3, 9, 10, 12, 15, 20, 26, 27, 29, 30 and 32-36 are believed to be allowable as depending from what are believed to be allowable independent claims 1, 14, 19 and 31 for the reasons given above. In addition, claims 2-3, 9, 10, 12, 15, 20, 26, 27, 29, 30 and 32-36 recite further limitations that distinguish over the applied art. In conclusion, it is respectfully submitted that claims 1-3, 9, 10, 12-15, 19, 20, 26, 27 and 29-36 are not anticipated nor rendered obvious by Rahman and are therefore allowable.

Rejection under 35 U.S.C. 103

The Examiner rejected claims 4-8, 11, 16-18, 21-25, 28 and 37 under 35 U.S.C. § 103(a) as being unpatentable over Rahman in view of Mokrytzki et al. (U.S. Patent No. 3,781,615), hereafter referred to as "Mokrytzki," or Maurio et al. (U.S. Patent No. 6,118,932), hereafter referred to as "Maurio," or Duba et al. (U.S. Patent No. 6,101,109), hereafter referred to as "Duba."

Specifically, the Examiner stated that

> The claims further recite inputting a carrier signal, inputting a modulating signal, and phase shift. However, the patents to Mokrytzki et al, Maurio et al, and Duba et al disclose plural inverters ripple current control comprising a carrier signal and phase shift. Prima facie case is made that Rahman et al disclose lead and lag signal modulation. It is known that the lead and lag signal modulation is the other term of phase shift and carrier signal. Since Rahman et al, Mokrytzki et al, Maurio et al, and Duba et al are plural inverters control systems for controlling the ripple current use for the same environment to reduce ripple current, it would have been obvious to one of ordinary skill in the art to provide Rahman et al with the carrier signal and phase shift technique as taught or suggested by Mokrytzki et al, Maurio et al, or Duba et al. It is inherent to have a phase shift in 30 degree, 60 degree, or 90 degree the way as recited in the claims.

Applicant respectfully traverses the rejection of claims 4-8, 11, 16-18, 21-25, 28 and 37 under 35 U.S.C. § 103(a).

Rahman is directed to a multiple inverter system as discussed in greater detail above.

Mokrytzki, as understood, is directed to a control method for transitioning a motor controller from PWM to non-PWM mode without creating a disruption of the motor modulation.

Maurio, as understood, is directed to a variable speed motor power supply converting ac power directly to ac power, without an intermediate dc link stage. Interleaving of carrier waveforms is done in order to control semiconductor switch means.

Duba, as understood, is directed to a static power converter which employs an unlimited number of modules connected in a particular multilevel, multi-phase, multi-circuit configuration. Interleaving of the carrier waveform is done between different levels of converter according to a specific algorithm that depends on the number of levels.

> "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

See Manual of Patent Examining Procedure, 8th Edition, Revision 6 (MPEP), Section 2143.03.

Applicant submits that dependent claims 4-8, 11, 16-18, 21-25, 28 and 37 are distinguishable from Rahman and/or Mokrytzki, Maurio or Duba for at least the following reasons. To begin, dependent claims 4-8, 11, 16-18, 21-25, 28 and 37 are believed to be distinguishable from Rahman and/or Mokrytzki, Maurio or Duba as depending from what are believed to be allowable independent claims 1, 14, 19 and 31 as discussed above. Furthermore, there is nothing in Mokrytzki, Maurio or Duba that teaches or suggests any of the limitations in independent claims 1, 14, 19 and 31 not taught or suggested by Rahman.

Therefore, in view of the above, dependent claims 4-8, 11, 16-18, 21-25, 28 and 37 are believed to be distinguishable from Rahman and/or Mokrytzki, Maurio or Duba and therefore are not anticipated nor rendered obvious by Rahman and/or Mokrytzki, Maurio or Duba. In addition, claims 4-8, 11, 16-18, 21-25, 28 and 37 recite further limitations that distinguish over the applied art. In conclusion, it is respectfully submitted that claims 4-8, 11, 16-18, 21-25, 28 and 37 are not anticipated nor rendered obvious by Rahman and/or Mokrytzki, Maurio or Duba and are therefore allowable.

CONCLUSION

In view of the above, Applicant respectfully requests reconsideration of the Application and withdrawal of the outstanding objections and rejections. As a result of the amendments and remarks presented herein, Applicant respectfully submits that claims 1-37 are not anticipated by nor rendered obvious by Rahman, Mokrytzki, Maurio or Duba ,or their combination, and thus, are in condition for allowance. As the claims are not anticipated by nor rendered obvious in view of the applied art, Applicant requests allowance of claims 1-37 in a timely manner. If the Examiner believes that prosecution of this Application could be expedited by a telephone conference, the Examiner is encouraged to contact the Applicant.

The Commissioner is hereby authorized to charge any additional fees and credit any overpayments to Deposit Account No. 50-1059.

Respectfully submitted,
McNEES, WALLACE & NURICK

/Brian T. Sattizahn/

By

Brian T. Sattizahn
Reg. No. 46,401
100 Pine Street, P.O. Box 1166
Harrisburg, PA 17108-1166
Tel: (717) 237-5258
Fax: (717) 237-5300

Dated: April 9, 2008